AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

On page 4, at line 8, please amend the paragraph as follows:

The sampling clock generator circuit for generating a sampling clock signal having frequency n times that of the external clock signal CLK on the receiving side in this case takes in the form of a PLL circuit utilizing a ring oscillator as a VCO (voltage controlled oscillator) as shown in FIG. 4. Outputs of n stages (when n is an even integer, n + 1 stages) of the ring oscillator are derived as the sampling clocks.

On page 11, at line 20, please amend the paragraph as follows:

In FIG. 1, which is a circuit construction of a data transmission system according to a first embodiment of the present invention, the data transmission system has a transmitting side (computer side) including a transmitting circuit 9 and a receiving side (liquid crystal device). The receiving side includes a serial-parallel converter 6, a data receiving circuit 7, a controller 8, a sampling clock generator circuit 11 in the form of a PLL control circuit including a phase comparator 2, a charge pump 3, a low-pass filter 4, a voltage follower 15, which is responsive to an output of a low-pass filter (LPF) 4 to generate a control voltage V_S, and a ring oscillator 12 composed of 2m series-connected inverters 12a and a delay line 13 for delaying a received external clock signal CLK, which is composed of 2m inverters 13a. The control voltage is applied to a power supply line 14 connected to the inverters 12a and 13a. Thus, an oscillation

frequency of the ring oscillator 12 is PLL-controlled such that it coincident with a frequency of the external clock signal CLK.

On page 18, at line 2, please amend the paragraph as follows:

The synthesizing ratio 1:4 is selected under assumption that the voltage for regulating the characteristics of the inverters 13a of the delay line 13 is about 20% of the voltage ~~VS~~ V_s of the power source line 14 of the ring oscillator 12 as a reference.